## REMARKS

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

By this amendment, claims 28-31 have been canceled. Therefore, claims 9-11, 16-19, and 24-27 are now pending.

Claims 9-11, 16-19, and 24-27 have been rejected under 35 U.S.C. 103 (a) as being unpatentable over Lasserre (US 6,760,829) in view of Sartorious (US 5,848,436). This rejection is traversed for the following reasons.

Each of independent claims 9, 16, and 19 recite an invention which allows sharing of data via memory access in half-word units (16-bit units) and byte units (8-bit unit) based on structure data. Contrary to the Examiner's assertion, lines 22-25 of column 9 of Lasserre do not disclose the storing of structure data, but merely describe the writing of a 16-bit value.

Lasserre does not disclose memory access in either 8 bit units or 16 bit units based on structure data. In Lasserre, since each endian processor does not perform reading or writing of structure data to allow communication with an opposite-endian processor, the address from the big-endian perspective and the address from the little-endian perspective are mismatched. As clearly stated in lines 22-25 of column 9 of Lasserre "[s]imilarly, writing the 16-bit value 0XFFEE to location 2 will overwrite 0XDDCC if the processor mode is little endian and 0xBBAA if it is big endian." As such, sharing of data via memory access in 8 bit units and 16 bit units is not possible in Lasserre, as opposed to the inventions recited in claims 9, 16, and 19 which allow data sharing via memory access in either 8 bit units or 16 bit units based on structure data (and as illustrated for example in Figs. 10A and 11A of the present application). In addition, although referred to by the Examiner, lines 63-65 in column 8 of Lasserre only describe that DSP 400 and CPU 402 share the memory 410, and there is no disclosure as to the configuration by which data sharing can be performed regardless of the units of the data.

In contrast, the present inventions recited in claims 9, 16, and 19 provide that each endian processor performs the reading or writing of structure data to allow communication with an opposite-endian processor. Thus, as explicitly recited in claims 9 and 16 "said first-endian processor

reads or writes the structure data to communicate with said second-endian processor, and said second-endian processor reads or writes the structure data to communicate with said first-endian processor" and in claim 19 the method comprises "causing the first-endian processor to read or write the structure data to communicate with the second-endian processor, and causing the second-endian processor to read or write the structure data to communicate with the first-endian processor." Accordingly, as shown for example in Fig. 10B and Fig. 11B of the present application, the mismatched addresses can be directly specified, and sharing of data regardless of whether it is in word units, half-word units, or byte units becomes possible.

Furthermore, in the fifth point of argument in the Response to Arguments section of the outstanding Office Action, the Examiner refers to lines 56-62 in column 8 of Lasserre. However, since the address from the big-endian perspective and the address from the little-endian perspective are mismatched, reading or writing of structure data to allow communication with an opposite-endian processor is not performed in Lasserre.

To further illustrate the difference between Lasserre and the present invention, please see the attached figures A-C, which graphically show the examples given by Lasserre with reference to Fig. 4 thereof. As is clearly apparent from Figs. A-C, since structure data definition is not described in Lasserre, the state shown in Figs. 11a and 12a of the present application arise and data sharing in half-word units (16-bit units) and byte units (8-bit units) is not possible. In contrast, in the present invention, since each endian processor performs the reading or writing of structure data to allow communication with an opposite-endian processor, mismatched addresses are directly specified, as shown in Figs. 11b and 12 b of the present application.

Moreover, the secondary reference, Sartorious, does not disclose the features of claims 9, 16, and 19 discussed in detail above, nor has the Examiner relied on Sartorious as providing such disclosure. Accordingly, no obvious combination of Lasserre and Sartorious would result in or otherwise render obvious the inventions recited in claims 9, 16, or 19 of the present application.

In view of the above, it is submitted that claims 9-11, 16-19, and 24-27 are allowable over the prior art of record and that the present application is in condition for allowance. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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